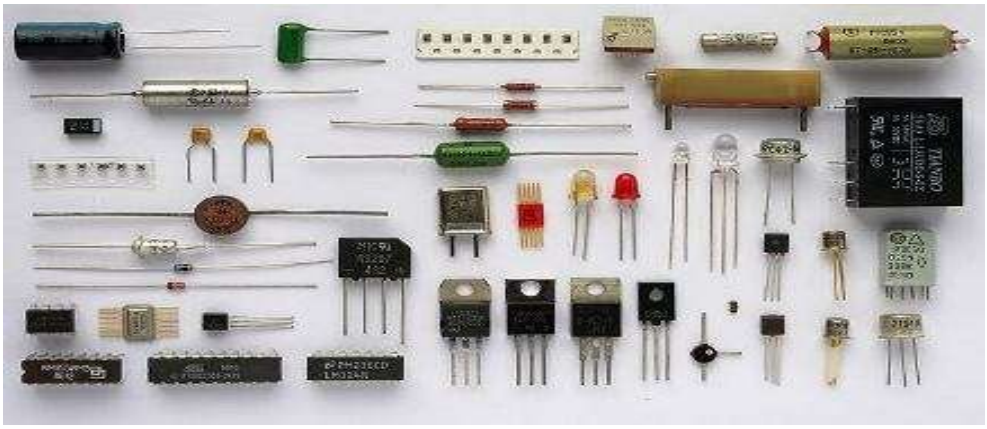
ANALOG ELECTRONIC CIRCUITS

LABORATORY MANUAL

III Semester (22ETL35)



Name of the Student	:
USN	:
Semester /Section	: *III –*
Batch	: *2025 - 26*

DAYANANDA SAGAR COLLEGE OF ENGINEERING

Accredited by National Assessment & Accreditation Council (NAAC) with 'A' Grade

(An Autonomous Institution affiliated to Visvesvaraya Technological University, Belagavi & ISO 9001:2008 Certified)

Telecommunication Engineering

Bangalore - 560078.

Vision of the Institute

To impart quality technical education with a focus on Research and Innovation emphasizing on Development of Sustainable and Inclusive Technology for the benefit of society.

Mission of the Institute

- To provide an environment that enhances creativity and Innovation in pursuit of Excellence.
- To nurture teamwork in order to transform individuals as responsible leaders and entrepreneurs.
- To train the students to the changing technical scenario and make them to understand the importance of Sustainable and Inclusive technologies.

Vision of the Department

- To disseminate quality technical education for achieving Academic Excellence through focused research and innovation encompassing contemporary technologies trends in electronic devices, telecommunication systems and standards for societal needful applications, of country in specific and global at broader perspective.

Mission of the Department

- By adopting quality curriculum design, associated with standard teaching learning process and assessment techniques; on par with standards for portability of graduates globally.
- By educating students towards contemporary technologies through consistent interaction with the leading industries based on the current socio-economic conditions of the society.
- By inculcating research attitude among graduates through lifelong learning in pursuit of academic excellence and career enrichment.

DAYANANDA SAGAR COLLEGE OF ENGINEERING

(An Autonomous Institution affiliated to Visvesvaraya Technological University, Belagavi)

Department of Telecommunication Engineering, Bengaluru-560078

ANALOG ELECTRONICS CIRCUITS LABORATORY (SYLLABUS)

III SEMESTER B. E (TE)

Course code: 22ETL35 **Credits: 02**
L: P: T: S: 0: 2: 0: 0 **CIE Marks: 50**
Exam Hours: 03 **SEE Marks: 50**
Total Hours: 32

Course Objectives:

This laboratory course enables students to

- Understand the electronic circuit schematic and its working
- Realize and test amplifier and oscillator circuits for the given specifications
- Realize the opamp circuits for the applications such as DAC, implement mathematical functions and precision rectifiers.
- Use the suitable ICs based on the specifications and functions.

Syllabus:

1. Wiring of RC coupled Single stage BJT/FET amplifier and determination of the gain-frequency response, input, and output impedances.
2. Design and set up the BJT/FET single stage common emitter voltage amplifier with feedback and determine the gain- bandwidth product, input and output impedances.
3. Wiring of BJT Darlington Emitter follower and determination of the gain, input and output impedances.
4. Testing of a transformer less Class – B push pull power amplifier and determination of its conversion efficiency.
5. Wiring and Testing for the performance of BJT/FET-RC Phase shift Oscillator for f0 ≤ 10 KHz.
6. Testing for the performance of BJT/FET-tuned oscillators – Hartley & Colpitt's Oscillators for RF range f0 ≥100KHz.
7. Testing for the performance of BJT/FET -Crystal Oscillator for f0 > 100 KHz.
8. Design a second order Active Filters using Operational Amplifier for the given cut-off frequency and to determine Roll-off from its frequency response.
i)Low pass filter ii) High pass filter.
9. Design 4-bit R – 2R Digital to Analog Converter using op-amp.
10. Design and test Monostable and Astable Multivibrator using 555 Timer.
11. Test the precision rectifiers using op-amp: i) Half wave rectifier ii) Full wave rectifier.
12. Design and set up the circuits using op-amp: Summing & Difference amplifier.

Course Outcomes:

After completion of the course, the graduates will be able to

CO1 Apply the fundamental knowledge of basic electronics in order to be well versed with the electronic components and circuits.

CO2 Demonstrate the small and large signal effects pertaining to active and passive components & design of BJT/FET circuits.

CO3 Analyze and evaluate the behaviour of various feedback concepts related to BJT/FET circuits.

CO4 Design and analysis of op-amp based applications like filters, rectifiers etc.

CO5 Design and analyse the basic electronic circuit experiments using 555 timers.

CO6 Understand the capabilities and limitations of analog circuits and make decisions regarding their best utilization in a specific situation.

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10. Design and Test Monostable and Astable Multivibrator using 555 Timer 37

Analog Electronic Circuits Lab

Cycle – I

1. Wiring of RC coupled Single stage BJT/FET amplifier and determination of the gain-frequency response, input, and output impedances.
2. Design and set up the BJT/FET single stage common emitter voltage amplifier with feedback and determine the gain- bandwidth product, input, and output impedances.
3. Wiring of BJT Darlington Emitter follower and determination of the gain, input and output impedances.
4. Testing of a transformer less Class – B push pull power amplifier and determination of its conversion efficiency.
5. Wiring and Testing for the performance of BJT/FET-RC Phase shift Oscillator for $f0 \leq 10$ KHz.
6. Testing for the performance of BJT/FET-tuned oscillators – Hartley & Colpitt's Oscillators for RF range $f0 \geq 100$KHz.
7. Testing for the performance of BJT/FET -Crystal Oscillator for $f0 > 100$ KHz.

Cycle - II

8. Design a second order Active Filters using Operational Amplifier for the given cut-off frequency and to determine Roll-off from its frequency response.
   i)Low pass filter ii) High pass filter.
9. Design 4-bit R – 2R Digital to Analog Converter using op-amp.
10. Test the precision rectifiers using op-amp: i) Half wave rectifier ii) Full wave rectifier.
11. Design and test Monostable and Astable Multivibrator using 555 Timer.
12. Design and set up the circuits using op-amp: Summing & Difference amplifier.

Important Instruction to Students

1. Students are expected to study Circuit, Theory, Procedure and Expected outputs before the conduction of any experiments.
2. Handle the Equipments Properly. Get yourself familiar with the Equipments mentioned in (3), (4) and (5).
3. Signal generator (To feed AC input to the Circuit):
    a. Set the shape of the waveform (sinusoidal),
    b. Set the frequency using coarse and fine adjustments.
    c. Set the offset adjustments. Set the CRO in DC mode and ensure the waveform is symmetry in both positive and negative cycle. If not, adjust it using the DC offsetting potentiometer.
    d. Set the voltage magnitude using V_{coarse} settings and V_{fine} adjustments.
4. CRO (To measure AC voltage and Frequency):
    a. Ensure that Channel selection and trigger mode are properly set.
    b. Select the right voltage and time scale to get the proper waveform
    c. For clipper and clamper circuits, observe the waveform in DC mode only
    d. Set the input waveform mainly for offset setting in DC mode only.
5. Multimeter (To measure Current (AC/DC), Voltage (AC/DC), Resistance etc.):
    a. Set the right mode before taking the readings. Wrong mode settings may damage the instrument.
    b. For current reading, connect the multimeter in mA (or A) mode to the circuit before switching on the supply. Do not remove the current meter when the supply is on. Check for ac and dc modes as required.
    c. For voltage reading ensure that proper ac or dc setting..
    d. Use the proper leads for the measurement. Wrong cables damage the instrument.
6. Rig up the circuit as per the circuit diagram, make sure for proper connections and finally energize the circuit with the supply.
7. While altering the circuit or checking out for an error in the circuit, Make sure that the power supply is turned off.

1. RC coupled Single stage BJT/FET amplifier

Aim:

To design RC Coupled single stage BJT amplifier and determine the gain, Frequency response, input and output impedance.

Apparatus Required:

Sl. No.	Components	Range	Quantity
1.	AFO	0-20V/10Hz-3Mhz	1
2.	VRPS	0 – 30V, 0-3A	1
3.	Resistor	12kΩ, 2.2kΩ, 470kΩ and 2.2kΩ	1 each
4.	Capacitor	1μF ,47μF	2,1
5.	NPN Transistor	SL100	1
6.	DRB		1
7.	Multimeter		1
8.	Bread Board		1
9.	Connecting Wires		10

Theory:

In RC coupled amplifier, the input capacitor is used to couple the input signal to the base of first transistor. Since the coupling from one stage to next stage can be achieved by a coupling capacitor followed by a connection to a shunt resistor, such amplifiers are called resistance capacitance (RC) coupled amplifiers. When an small signal is applied to the input of the first stage it is amplified with a phase reversal by the transistor. The frequency response is a graph of the gain (in decibels) versus the frequency (in logarithmic scale). This characteristic can be subdivided into low, medium and high frequency regions. In the low frequency range, the gain drops due to increasing reactance of coupling capacitor, source capacitance and emitter capacitor. As the frequency increases, the capacitive reactance reduces and the gain increases. After this if the frequency is increased further, i.e. in the high frequency range, the gain drops due to the increased flow of the AC signal through CE. To fix the boundaries of frequency where the gain is relatively high and constant, $0.707A_{mid}$ is chosen to be the voltage gain at the cut-off levels. The corresponding frequencies f1 and f2 are generally called the corner, cut-off,

band, break or half power frequencies. The multiplier 0.707 is chosen because at this level the output power is half the mid-band power output. This is illustrated in the model graph.

Circuit Diagram:

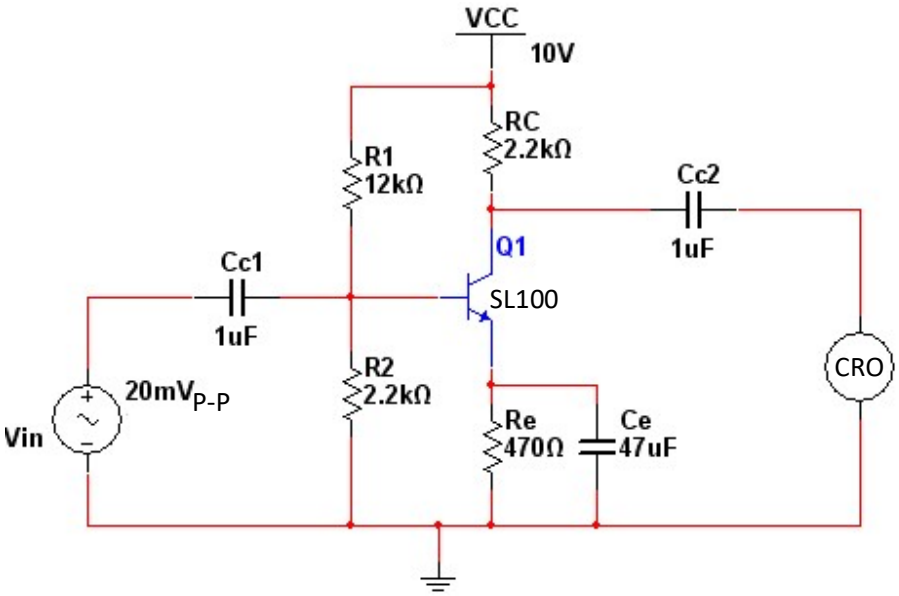


Fig.1.1: RC Coupled Amplifier

Design:

a. To find R_E

Let V_{CC} = 10V, $I_E = I_C$ = 2mA and β = 100 (for SL100)

Choose $V_{CE} = \frac{V_{CC}}{2}$ = 5V (to put the transistor in active region)

Consider $V_{RE} = \frac{1}{10} V_{CC}$ = 1V

$V_{RE} = I_E R_E$

Therefore $R_E = \frac{V_{RE}}{I_E}$ = 500Ω. (Select 470Ω)

b. To find R_C

$V_{CC} = I_C R_C + V_{CE} + V_{RE}$

$10 = I_C R_C + 5 + 1$

Therefore, $R_C = \frac{10-6}{2mA}$ = 2kΩ (Choose 2.2kΩ)

C. To find R_1 & R_2

Apply KVL to the input loop

$V_{R2} = V_{BE} + V_{RE} = 0.6 + 1 = 1.6V$

Also $V_{R2} = R_2 * \frac{V_{CC}}{R_1 + R_2} \Rightarrow \frac{R_2}{R_1 + R_2} = 0.16$

Choose $R_2 = 2.2k\Omega$

Then $R_1 = 12k\Omega$.

d. To design bypass Capacitor (C_E)

Let $X_{CE} = 0.1\ R_E \Rightarrow 0.1 * 470 = 47\Omega$

Therefore $C_E = \frac{1}{2*\pi*X_{CE}} \approx 33.8\mu F$ (Choose $47\mu F$).

Procedure:

1. The connections are made as per the fig. 6.1.
2. Check for the DC conditions by setting $V_{CC} = 10V$. V_{CE} Should is approximately equal to 5V.
3. Apply a small signal input of around $20mV_{P-P}$ signal. Keep the input signal a constant, vary the frequency over a wide range (from 100Hz to 1MHz) and tabulate the output voltage of the amplifier.
4. Calculate the gain of the amplifier by

Gain in dB = $20 \log_{10} \frac{V_0}{V_{in}}$

5. Plot the frequency vs. Gain in a semi log sheet and calculate the bandwidth of the amplifier.

Tabulation:

V_{in} = 20 mV_{p-p}

Frequency in Hz	V_0 in Volts	$A_V = \frac{V_0}{V_{in}}$	Gain in dB =20 $\log_{10} \frac{V_0}{V_{in}}$

Model Graph:

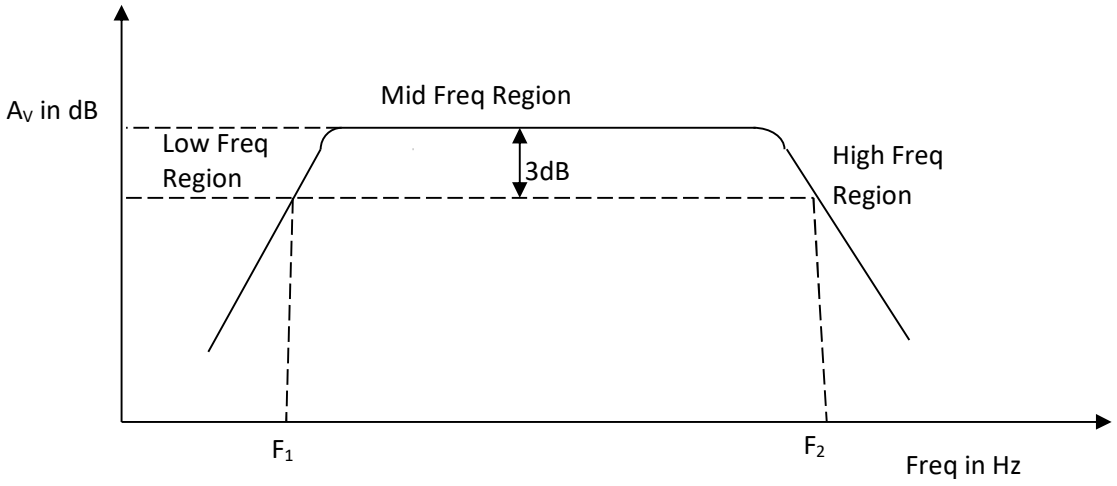


Fig.1.2. Frequency response curve of RC Coupled Amplifier

To measure input impedance (Z_i):

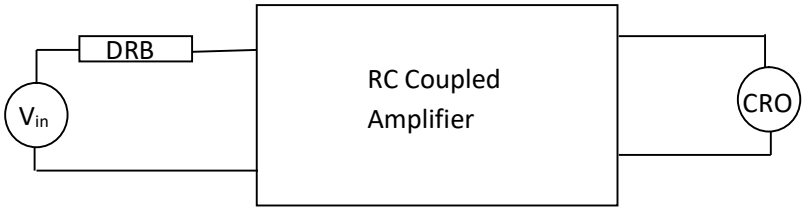


Fig.1.3: Circuit to measure Z_i

1. DRB is connected as shown in the fig.6.3 and DRB is set to 0Ω.
2. V_{in} of 20mV is applied to the Amplifier choosing a mid band Frequency (say 10 kHz).
3. Note the output amplitude (V_0) and increase the DRB till V_0 reduces to half of its value.
4. This DRB value gives the input impedance Z_i of the RC Coupled amplifier.

TO measure output impedance (Z_0):

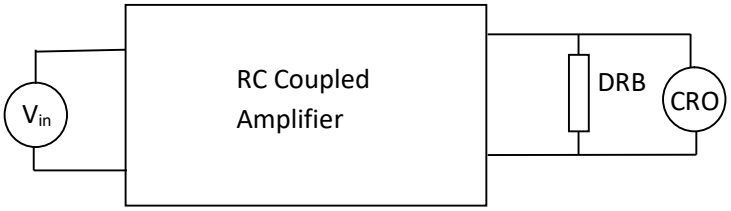


Fig.1.4: Circuit to measure Z_0

1. DRB is connected as shown in the fig.6.4 and DRB is set to Maximum value.
2. V_{in} of 20mV is applied to the Amplifier choosing a mid band Frequency (say 10 kHz).
3. Note the output amplitude (V_0) and decrease the DRB till V_0 reduces to half of its value.
4. This DRB value gives the input impedance Z_0 of the RC Coupled amplifier.

Results:

Thus the RC Coupled amplifier using BJT amplifier is designed and the following parameters are determined.

Bandwidth:

Mid band Gain = A_{MID}:

Input Impedance (Z_i):

Output Impedance (Z_0):

2. Darlington Emitter Follower

Aim:

To design BJT Darlington Emitter Follower without bootstrapping and to determine gain, input and output impedances.

Components Required:

Sl.No.	Components	Range	Quantity
1.	AFO	0-20V/10Hz-3Mhz	1
2.	DC Power Supply	0 – 30V	1
3.	Resistor	1MΩ,1.5MΩ,10kΩ and 1.2k Ω	1 each
4.	Capacitor	0.1μF and 10μF	2,1
5.	NPN Transistor	SL100	2
6.	DRB		1
7.	Multimeter		1
8.	Bread Board		1

Theory:

The emitter follower has reasonably high input impedance and may be used wherever input impedance up to about 500kΩ is needed. For higher input impedance, we may use 2 transistors to form what is called a Darlington pair. When the output is taken from the Emitter terminal of the transistor, the network is referred to as an Emitter follower. The output voltage is always less than the input voltage due to the drop between the base and emitter. However, the voltage gain is usually approximated to one. In addition, the output is having the same polarity as the input voltage. Hence it is said to follow the input voltage with an in-phase relationship. This accounts for the terminology 'Emitter – follower'. For ac analysis, the collector is grounded, therefore the circuit is actually a common-collector configuration. This circuit presents high impedance at the input and low impedance at the output. It is therefore frequently used for impedance matching purposes, where a load is matched to the source impedance for maximum signal transfer through the system.

The Darlington connection shown is a connection of two transistors whose result is a current gain that is the product of the current gains of the individual transistors. Hence

the Darlington pair operates as one 'Super beta' transistor offering a very high current gain. Thus the Darlington Emitter follower is a CC configuration that has the following characteristics:

Voltage gain → almost unity

Current gain → very high, a few thousands

Input impedance → high, hundreds of Kilo ohms

Output impedance → low, tens of ohms

Darlington Emitter follower with Bootstrap

The biasing network reduces the input impedance of the amplifier. This is because of the considerable amount of current it takes. By h-parameter model input impedance is the parallel combination of input resistance of the transistor and of the biasing network. The biasing network resistance is always less than the resistance of the transistor. To improve the resistance of the circuit, a series circuit consisting of a resistor and a capacitor is connected between the emitter and the base. This process of connecting output to input through a resistor under AC conditions is called Bootstrapping.

Circuit Diagram:

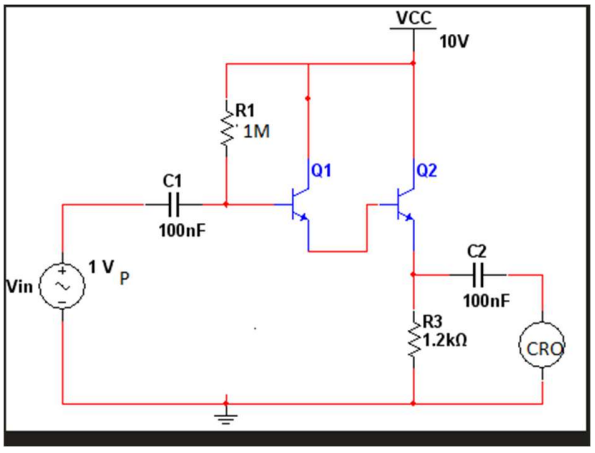


Fig.2.1: Darlington Emitter Follower without Bootstrap

Design:

Let V_{CC} = 10V, $I_E = I_{C2}$ = 4mA and β = 100 (for SL100)

Choose $V_{CE} = \frac{V_{CC}}{2}$ = 5V (to put the transistor in active region)

a. To find R_E

Appling KVL for the output circuit

$V_{CC} = V_{CE2} + I_{c2} R_E$

$R3 = R_E = \frac{V_{CC} - V_{CE2}}{I_{C2}} = \frac{10-5}{4m} = 1.25k\Omega \approx 1.2k\Omega$

b. To find R_1 and R_2

Let $I_{B2} = \frac{I_{C2}}{\beta} = 0.04mA$

$I_{B1} = \frac{I_{C1}}{\beta} = 0.4\mu A$

Let $I_1 = 10\ I_{B1} = 10*0.4\mu A = 4\mu A$

$I_2 = 9\ I_{B1} = 9*0.4\mu A = 3.6\mu A$

$R_2 = \frac{V_{R2}}{I_2} = \frac{V_{RE} + V_{BE1} + V_{BE2}}{I_2} = \frac{5+0.6+0.6}{3.6m} = 1.7M\Omega \approx 1.5M\Omega$

Now $R_1 = \frac{V_{R1}}{I_2} = \frac{10-6.2}{4m} = 0.75M\Omega \approx 1M\Omega$

Procedure:

1. The connections are made as per the fig. 7.1.
2. Check for the DC conditions by setting V_{CC} = 10V. V_{CE} Should is approximately equal to 5V.
3. Apply an input of around $1V_{P-P}$ signal. Keep the input signal a constant, vary the frequency over a wide range (from 100Hz to 1MHz) and tabulate the output voltage of the circuit.
4. Calculate the gain of the amplifier by

Gain in dB = $20 \log_{10} \frac{V_0}{V_{in}}$ (Should be one for a Voltage follower circuit).

5. Find the input and output impedance as explained below.

To measure input impedance (Z_i):

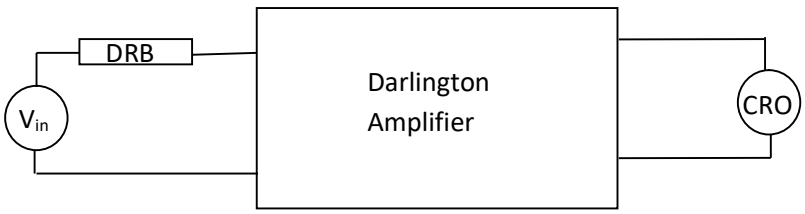


Fig.2.2: Circuit to measure Z_i

1. DRB is connected as shown in the fig.7.2 and DRB is set to 0Ω.
2. V_{in} of $1V_{p-p}$ is applied to the Amplifier choosing a mid band Frequency (say 10 kHz).
3. Note the output amplitude (V_0) and increase the DRB till V_0 reduces to half of its value.
4. This DRB value gives the input impedance Z_i of the Darlington amplifier.

To measure output impedance (Z_0):



Fig.2.3: Circuit to measure Z_0

1. DRB is connected as shown in the fig.7.3 and DRB is set to Maximum value.
2. V_{in} of $1V_{p-p}$ is applied to the Amplifier choosing a mid band Frequency (say 10 kHz).
3. Note the output amplitude (V_0) and decrease the DRB till V_0 reduces to half of its value.
4. This DRB value gives the input impedance Z_0 of the Darlington amplifier

Tabulation:

V_{IN} = $1V_{P-P}$

Frequency in Hz	V_0 in Volts	$A_V = \frac{V_0}{V_{in}}$	Gain in dB =20 $\log_{10} \frac{V_0}{V_{in}}$

Results:

Thus the Darlington amplifier using BJT amplifier is designed and the following amplifier parameters are determined.

Amplifier Parameter	Without Bootstrap
Voltage Gain (A_V)	
Input Impedance (Z_i)	
Output Impedance (Z_0)	

3. Transformer Less Class-B Push-Pull Power Amplifier

Aim:

To test class-B transformer less push pull amplifier for crossover distortion and find its conversion efficiency.

Components required:

Sl.No	Components	Range	Quantity
1	AFO	0-20V/10Hz-3Mhz	1
2.	VRPS	0 – 30V, 0-3A	2
3.	Resistor	10kΩ	1
4.	Capacitor	0.1μF	2
5.	Transistors	SL100 & SK100	1 each
6.	Multimeter		1
7.	CRO		1
8.	Connecting Wires		10

Theory:

It is basically a class –B amplifier, in which a transistor conducts for a half cycle. For complete conduction, such an amplifier uses two transistors. During the positive half cycle of the input signal, the NPN transistor conducts and during the negative half cycle PNP transistor conducts. Since one part of the circuit pushes the signal high during one half-cycle of the output and the other part pulls the signal low during the other half-cycle, this circuit is referred as Push-pull amplifier. The transistors conduct only if the input voltage crosses the threshold voltage of 0.7v.During this interval no transistors conducts .This causes a distortion called crossover distortion.

Procedure:

1. Rig up the circuit as per the fig.8.1

2. Since it is a large signal amplifier, the input signal in terms of volts is given and output should be an undistorted sine wave.

3. The input amplitude is increased further till we notice distortion at the output.

4. The Conversion efficiency (η) is calculated as

$$\text{Conversion efficiency } (\eta) = \frac{\pi V_{L(PEAK)}}{4 * V_{CC}} * 100 \text{ (Ideal conversion efficiency = 78\%)}$$

Circuit Diagram:

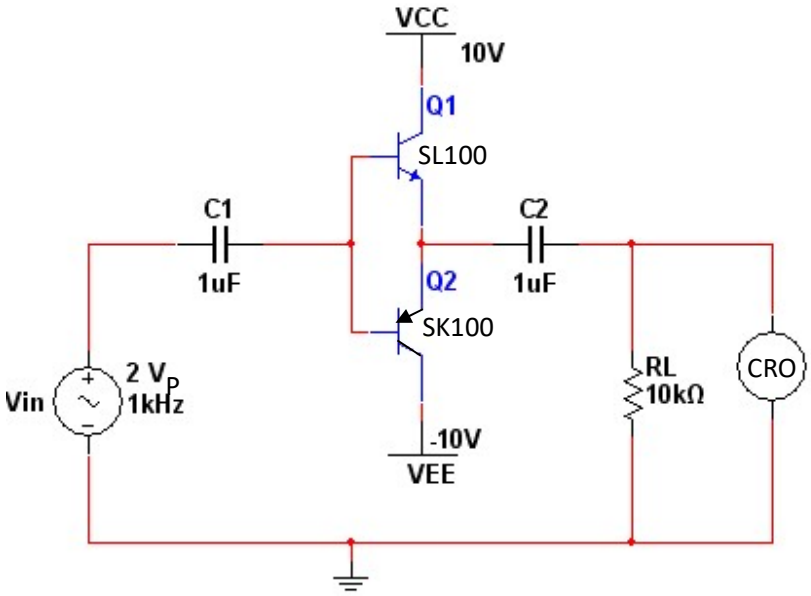


Fig.3.1: class-B Push-pull Amplifier

Observations:

$V_{L\ (Peak)}$ =…….V

V_{CC} = 10V

∴ Conversion Efficiency (η) = ……%

Output Waveform:

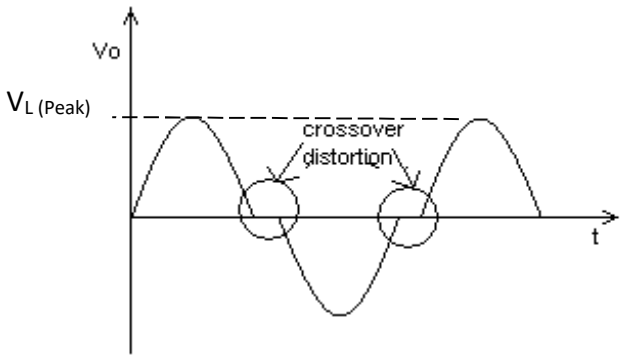


Fig.3.2: Cross over Distortion output.

Result:

Thus the class-B transformer less push pull amplifier for crossover distortion is tested and its conversion efficiency is determined.

Conversion Efficiency (η) = ……%

4. Multi Stage Voltage Feedback Amplifier

Aim:

To plot the frequency response of a multistage amplifier with and without feedback and to find input impedance, output impedance and voltage gain.

Components Required:

Sl.No.	Components	Range	Quantity
1.	VRPS	0 – 30V, 0-3A	1
2.	Resistor	As per Design	
3.	NPN Transistor	SL100	2
4.	Capacitor	0.47μF, 47 μF	3, 2
5.	Multimeter		1
6.	CRO		1
7.	Bread Board/Spring Board		1
8.	Connecting Wires		10

Theory:

A **negative feedback amplifier** (or **feedback amplifier**) is an electronic amplifier that subtracts a fraction of its output from its input, so that negative feedback opposes the original signal. The applied negative feedback improves performance (gain stability, linearity, frequency response, step response) and reduces sensitivity to parameter variations due to manufacturing or environment. Because of these advantages, many amplifiers and control systems use negative feedback.

Negative feedback trades gain for higher linearity (reducing distortion), and can provide other benefits.

Pros:

- Can increase input impedance
- Can decrease output impedance
- Reduces distortion (increases linearity)
- Increases the bandwidth
- Desensitizes gain to component variations
- Can control step response of amplifier

Cons:

- May lead to instability if not designed carefully
- Amplifier gain decreases
- Input and output impedances of a negative feedback amplifier (*closed-loop amplifier*) become sensitive to the gain of an amplifier without feedback (*open-loop amplifier*)—that exposes these impedances to variations in the open loop gain, for example, due to parameter variations or nonlinearity of the open-loop gain.

Circuit Diagram:

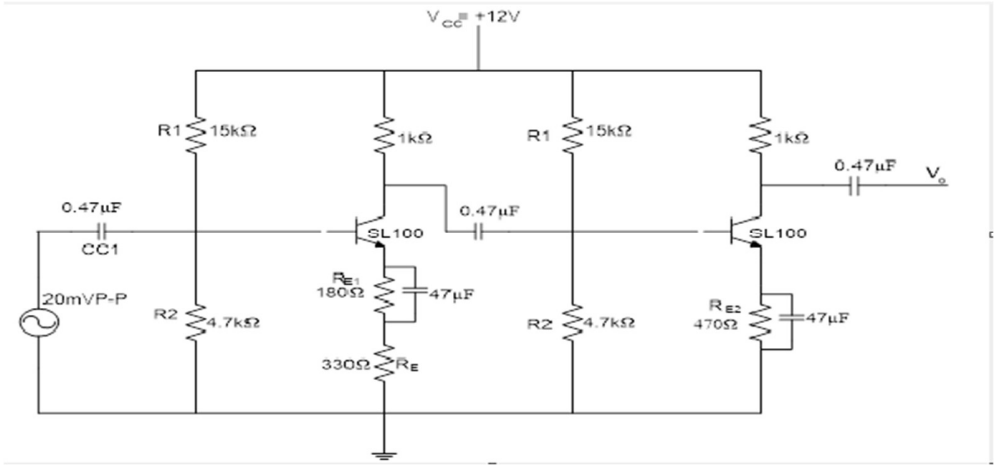


Fig 4.1: Multi Stage Voltage Amplifier- Without Feedback

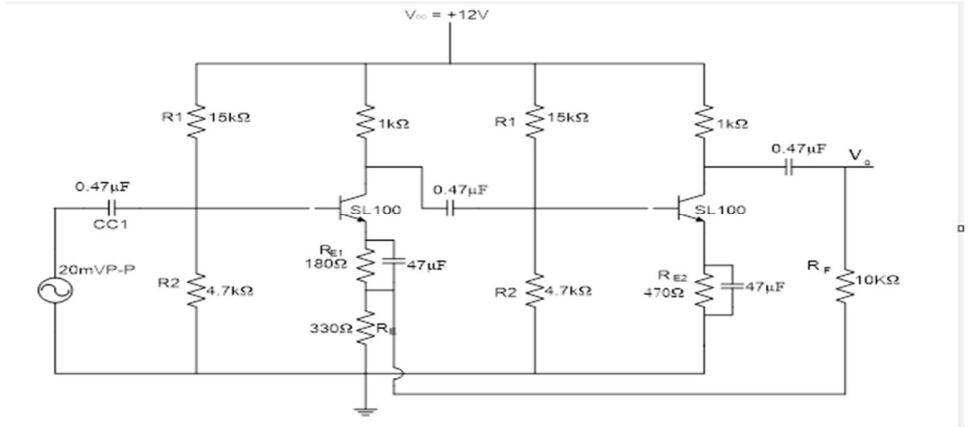


Fig 4.2: Multi Stage Voltage Amplifier- With Feedback

Design:

Let V_{CC} = 12 V, I_C = 4mA, V_{CE} = 6V

$V_E = \frac{VCC}{6}$ = 2V.

Let $CC_1 = CC_2 = CC_3 = 0.47\mu F$. and $CE_1 = CE_2 = 47\mu F$.

$V_E = I_E R_E$

$R_E = \frac{2V}{4mA} = 0.5k\Omega$

Since $I_E = I_C$, $R_E = 500\Omega$ (Use 470Ω)

1st stage, Split R_E into 2 parts:

$R_E = 330\Omega + 180\Omega$

KVL to CE loop,

$V_{CC} - I_C R_C - V_{CE} - V_E = 0$

$R_C = \frac{12-6-2}{4m} = 1K\Omega$

$V_B = \frac{V_{CC}\ R_2}{R_1+R_2} => \frac{0.7+2}{12} = \frac{R_2}{R_1+R_2}$

Simplifying $R_2 = 0.29\ R_1$

Let $R_2 = 4.7K\Omega$, => $R_1 = 16.18K\Omega$ (Use $15K\Omega$)

2nd stage design is same as that of 1st stage Amplifier design.

Feedback Factor $\beta = \frac{R'_E}{R_F + R'_E}$

R_F should be much greater than R_C. β should be between 0.01 to 0.1.

Let $R_F = 10K\Omega$,

So, $\beta = \frac{330}{330+10K} = 0.032$

Procedure:

1. The amplifier is rigged as per the circuit and DC condition is checked. i.e., $V_{CE} = 5V$.
2. After DC condition is checked, the entire circuit is rigged up.
3. Connect AC source keeping AC source in mid band frequency region.
4. Keeping input amplitude a constant, vary the frequency in suitable steps and note the corresponding amplitude.
5. Calculate Av in decibels and plot the frequency response and determine the bandwidth(BW)

To measure input impedance (Z_i):

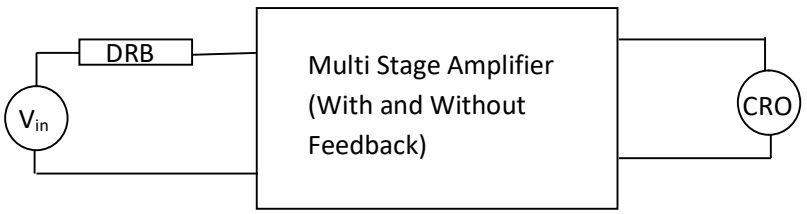


Fig.4.3: Circuit to measure Z_i

1. DRB is connected as shown in the fig.9.3 and DRB is set to 0Ω.
2. V_{in} of $20mV_{p-p}$ is applied to the Amplifier choosing a mid band Frequency (say 10 kHz).
3. Note the output amplitude (V_0) and increase the DRB till V_0 reduces to half of its value.
4. This DRB value gives the input impedance Z_i of the multistage amplifier.

To measure output impedance (Z_0):

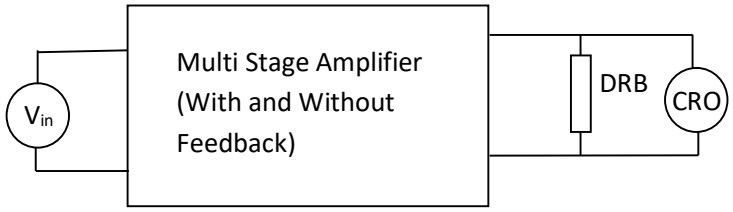


Fig.4.4: Circuit to measure Z_0

1. DRB is connected as shown in the fig.9.4 and DRB is set to Maximum value.
2. V_{in} of $20mV_{p-p}$ is applied to the Amplifier choosing a mid band Frequency (say 10 kHz).
3. Note the output amplitude (V_0) and decrease the DRB till V_0 reduces to half of its value.
4. This DRB value gives the input impedance Z_0 of the multistage amplifier.

Tabulation:

$V_i = 20mV_{P-P}$

Frequency in Hz	**V_o in Volts**	**Av = $\frac{V_O}{V_i}$**	**Gain in dB = $20\log A_V$**

Model Graph:

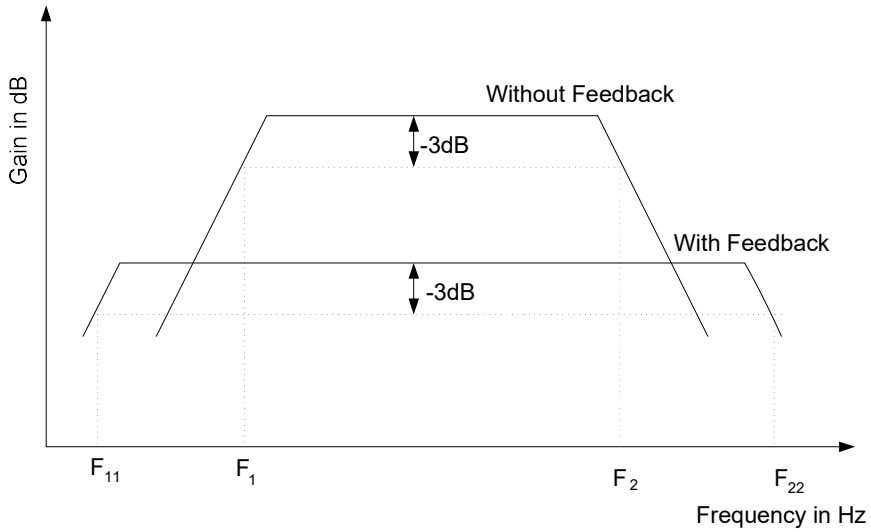


Fig: 9.5: Frequency response of multistage voltage amplifier

Result:

Thus the multistage voltage series amplifier with and without feedback is performed and following parameters are tabulated.

Parameters	Without feedback	With feedback
Av		
Bandwidth		
Input Impedance		
Output Impedance		

5. RC Phase Shift Oscillator

Aim:

To test the performance of BJT-RC Phase shift Oscillator for F = 5 KHz

Components Required:

Sl.No.	Components	Range	Quantity
1.	VRPS	0 – 30V, 0-3A	1
2.	Resistor	12kΩ, 2.2kΩ, 470kΩ and 2.2kΩ	1 each
3.	Resistor	1kΩ, 1kΩ Pot	2 each
4.	Capacitor	1μF ,47μF	2,1
5.	NPN Transistor	SL100	1
6.	Capacitor	0.01μF	3
7.	Multimeter		1
8.	CRO		1
9.	Bread Board		1
10.	Connecting Wires		10

Theory:

RC phase shift Oscillator basically consists of an amplifier and feedback network consisting of resistors and capacitors in ladder fashion.

The current I is in phase with V_0, whereas the capacitor voltage V_C lags the current I by φ. (90°→Ideal value).or the output voltage V_O leads the I/P voltage V_I by angle φ is adjusted in practice, equal to 60°. RC network is used in feedback path. In Oscillator, feedback network must introduce a phase shift of 180° to obtain total phase shift around a loop as 360°.Thus three RC network each provide 60° phase shift is cascaded, so that it produces total 180° phase shift.

Design:

Design of Amplifier is same as RC Coupled Amplifier

Design of RC Network:

$F_0 = \frac{1}{2\pi RC\sqrt{6+4}}$ where $k = \frac{R_C}{R} = 2.2$

Let F_0 = 5kHz and C = 0.01μF

Then R = 1.2kΩ (Select 1kΩ)

Circuit Diagram:

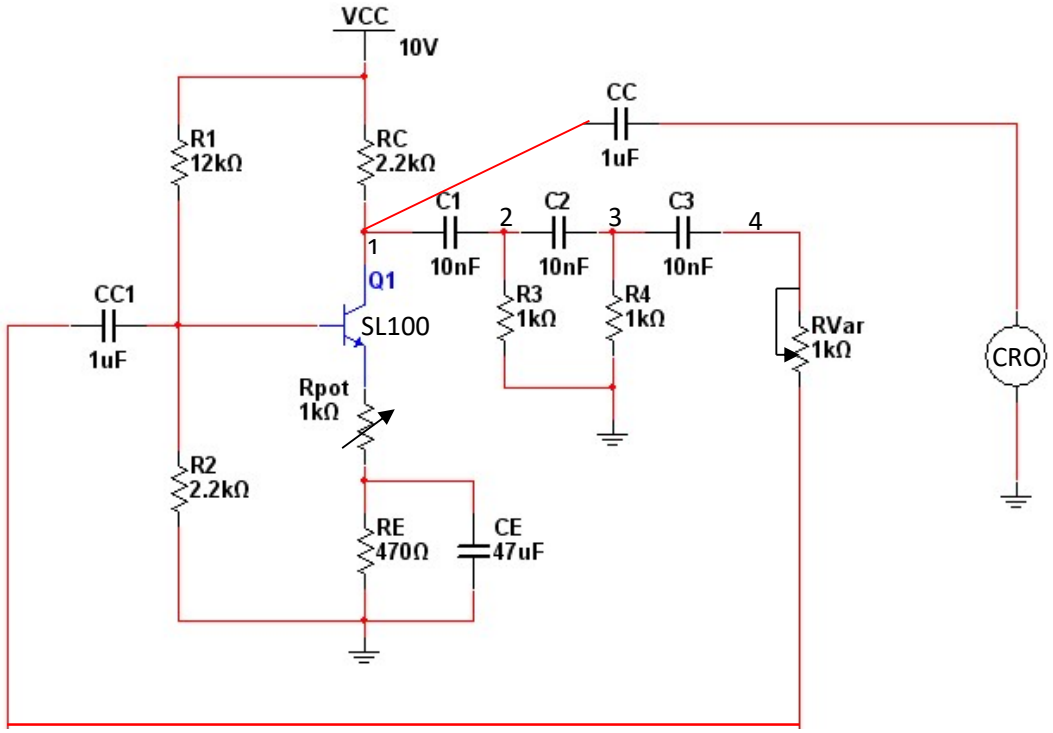


Fig.5.1: RC Phase Shift Oscillator

Procedure:

1. The amplifier is rigged as per the circuit and DC condition is checked. i.e., V_{CE} = 5V.

2. After DC condition is checked, the entire circuit is rigged up.

3. CRO has to be connected between point 1 and ground to observe sinusoidal waveform.

4. For undistorted output, the 1kΩpot is varied suitably and frequency and amplitude of the output is noted.

Expected Waveforms:

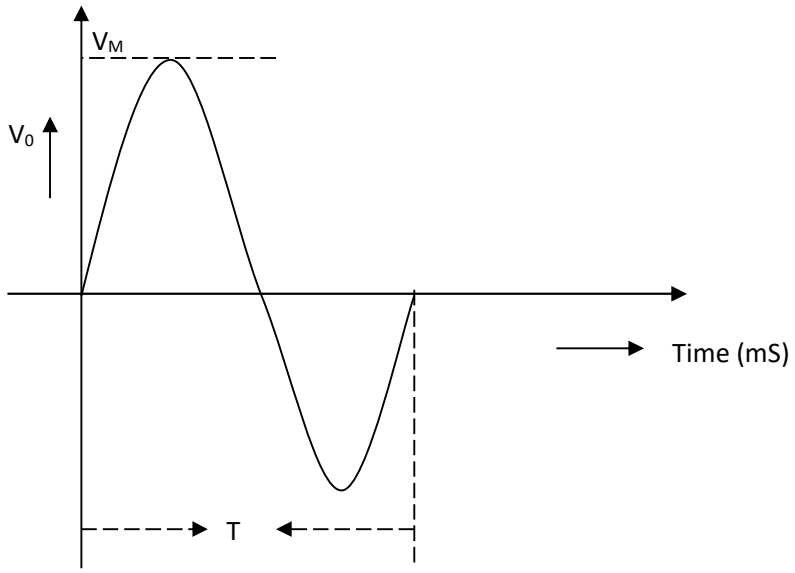


Fig.5.2: Output waveform.

Observations:

$F_{pract} = \frac{1}{T}$ = ...Hz

V_M = ...Volts

Result:

Thus the performance of BJT-RC phase shift oscillator is tested for a frequency of 5 kHz.

6. Hartley and Colpitts Oscillator

Aim:

To Test the performance of BJT – Hartley & Colpitt's Oscillators for RF range $f_0 \geq 100KHz$.

Components required:

Sl.No.	Components	Range	Quantity
1.	VRPS	0 – 30V, 0-3A	1
2.	Resistor	12kΩ, 2.2kΩ, 470kΩ and 2.2kΩ	1 each
3.	Capacitor	1μF ,47μF	2,1
4.	NPN Transistor	SL100	1
5.	DRB		1
6.	DCB & DIB		2 each
7.	Multimeter		1
8.	CRO		1
9.	Bread Board		1
10.	Connecting Wires		10

Theory:

In phase shift oscillator, RC circuit is used to get the oscillation whose frequency is in the audio range. To get higher frequency of oscillation, feedback circuit to have inductor and capacitors. The oscillators that employ L&C elements are called tuned oscillators.

Hartley and Colpitts oscillators belong to LC tuned oscillator. A Hartley oscillator as shown in fig.11.1 has a Potential divider biased BJT amplifier and LC feedback circuit. Its feedback or tank circuit consists of two inductor in series and one capacitor in parallel. Colpitts oscillator is similar to the Hartley oscillator except the change in the tank circuit. Here the tank circuit consists of two capacitors in series and one capacitor as shown in fig.11.2

The amplifier is single stage amplifier and has 180 degree phase shift. So this tank circuit provides 180 degree phase shift due to inductor & capacitor connection to make total phase shift of the circuit as 360 degree at the frequency of oscillation. When the feedback is adjusted so that $A\beta = 1$, sustained oscillation occurs at the output.

Frequency of the oscillation is $F_0 = \frac{1}{2\pi\sqrt{LC}}$

In the case of Hartley oscillator L = L1+L2

In the case of Colpitts Oscillator C = $\frac{C_1C_2}{C_1+C_2}$

Design:

Biasing circuit design for BJT amplifier:-

Use the same biasing circuit used for RC Phase Shift Oscillator.

Tank Circuit design of Hartley Oscillator:

Let F_0 = 100 kHz.

Assume $L_{eq} = L_1 + L_2$ =2mH

Calculate C

C = $1/((100k)^2 (2\pi)^2 2mH) = 1.26nF \approx 1nF$

Tank Circuit design of Colpitts Oscillator:

Let C_1 = 0.1μF and C_2 = 0.001μF

$\therefore C_{EQ}$ = 0.99nF

Calculate L:

L = $1/((100k)^2(2\pi)^2 0.99nF) =2.5mH$

Procedure:

1. The amplifier circuit is rigged up as shown in the diagram and the DC condition is checked. i.e., V_{CE} = 5V
2. Also observe the wave form across the output using CRO
3. If wave is not observed, adjust the variable 1K pot in series with R_E resistor, until an undistorted sine wave is obtained.
4. Draw the waveform on the graph sheet and note down the frequency.

Circuit Diagrams:

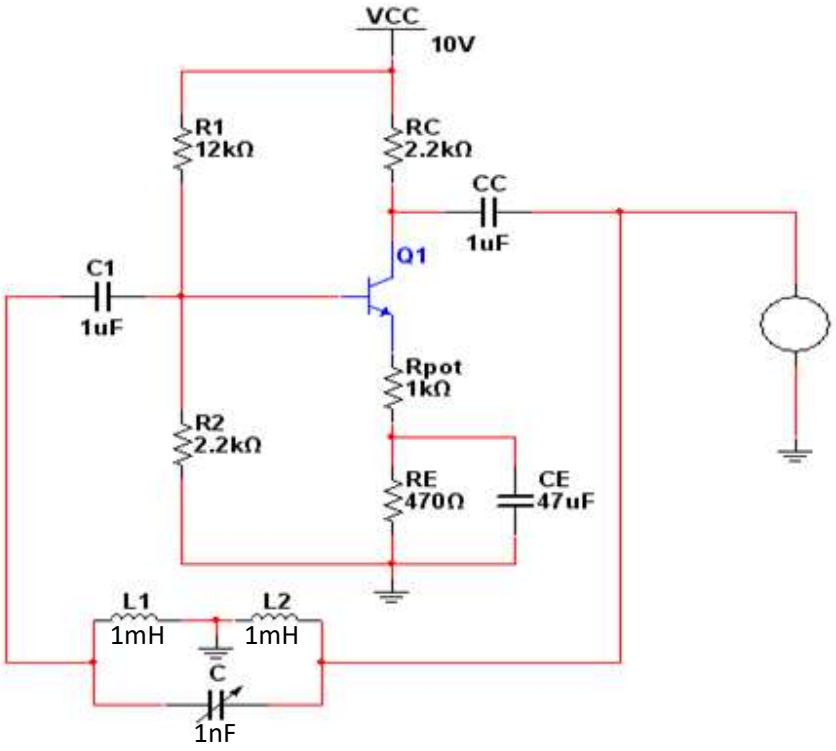


Fig.6.1 Hartley Oscillator

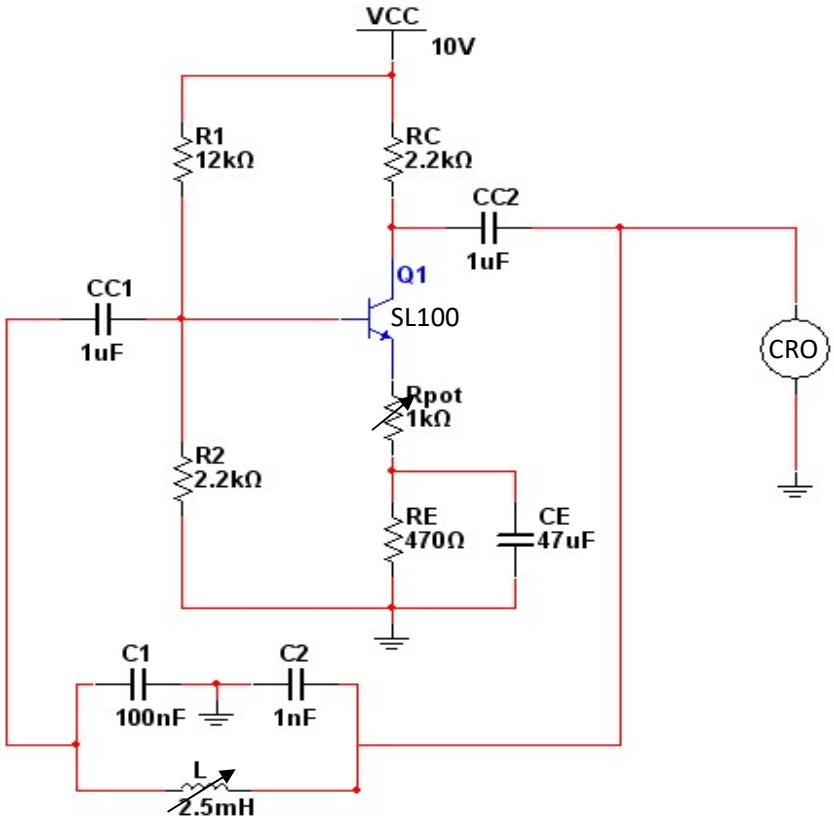


Fig.6.2: Colpitts Oscillator

Expected output:

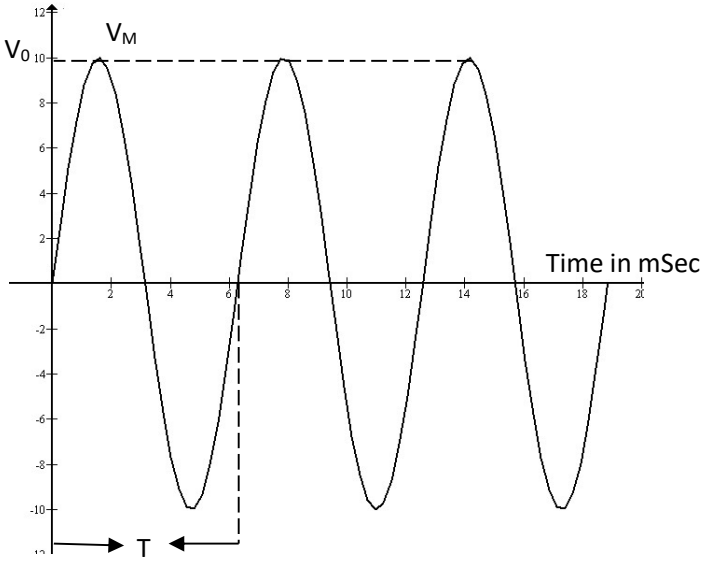


Fig.6.3: RF output from oscillator

Observations:

For Hartley Oscillator	**For Colpitts Oscillator**
Time: ……mSec	Time: ……mSec
Frequency:……Hz	Frequency:……Hz

Result:

Thus the performance of BJT – Hartley & Colpitt's Oscillators for RF range $f_0 \geq 100$KHz is studied.

7. Crystal Oscillator

Aim:

To design and test the performance of BJT crystal oscillator for a frequency F_0 >100 kHz.

Components required:

Sl.No.	Components	Range	Quantity
1.	VRPS	0 – 30V, 0-3A	1
2.	Resistor	22kΩ,4.7kΩ, 1kΩ and 220Ω	1 each
3.	Capacitor	0.1μF , 0.47μF and 47 μF	1 each
4.	NPN Transistor	SL100	1
5.	Potentiometer	1kΩ	1
6.	Crystal	2MHz	1
7.	Multimeter		1
8.	CRO		1
9.	Bread Board		1
10.	Connecting Wires		10

Theory:

One of the most important features of an oscillator is its Frequency Stability, or in other words its ability to provide a constant frequency output under varying conditions. Some of the factors that affect the frequency stability of an oscillator include: temperature, variations in the load and changes in the power supply. Frequency stability of the output signal can be improved by the proper selection of the components used for the resonant feedback circuit including the amplifier but there is a limit to the stability that can be obtained from normal LC and RC tank circuits. For very high stability a quartz crystal is generally used as the frequency determining device to produce other types of oscillator circuit known generally as Crystal Oscillators**.**

A quartz crystal has a resonant frequency similar to that of a electrically tuned tank circuit but with a much higher Q factor due to its low resistance, with typical frequencies ranging from 4kHz to 10MHz.

In a Crystal Oscillator circuit the oscillator will oscillate at the crystals fundamental series resonant frequency as the crystal always wants to oscillate when a voltage source is applied to it. However, it is also possible to "tune" a crystal oscillator to any even harmonic of the fundamental frequency, (2nd, 4th, 8th etc.) and these are known generally as Harmonic Oscillators while Overtone Oscillators vibrate at odd multiples of the fundamental frequency, 3rd, 5th, 11th etc). Generally, crystal oscillators that operate at overtone frequencies do so using their series resonant frequency.

Design:

a. To find R_E

Let V_{CC} = 10V, $I_E = I_C$ = 2mA and β = 100 (for SL100)

Choose $V_{CE} = \frac{V_{CC}}{2}$ = 5V (to put the transistor in active region)

Consider $V_{RE} = \frac{1}{10} V_{CC}$ = 1V

$V_{RE} = I_E R_E$

Therefore $R_E = \frac{V_{RE}}{I_E}$ = 500Ω. (Select 470Ω)

b. To find R_C

$V_{CC} = I_C R_C + V_{CE} + V_{RE}$

$10 = I_C R_C + 5 + 1$

Therefore, $R_C = \frac{10-6}{2mA}$ = 2kΩ (Choose 2.2kΩ)

C. To find R_1 & R_2

Apply KVL to the input loop

$V_{R2} = V_{BE} + V_{RE} = 0.6 + 1 = 1.6V$

Also $V_{R2} = R_2 * \frac{V_{CC}}{R_1 + R_2} \Rightarrow \frac{R_2}{R_1 + R_2} = 0.16$

Choose R_2 = 4.7kΩ

Then R_1 = 22kΩ.

Circuit diagram:

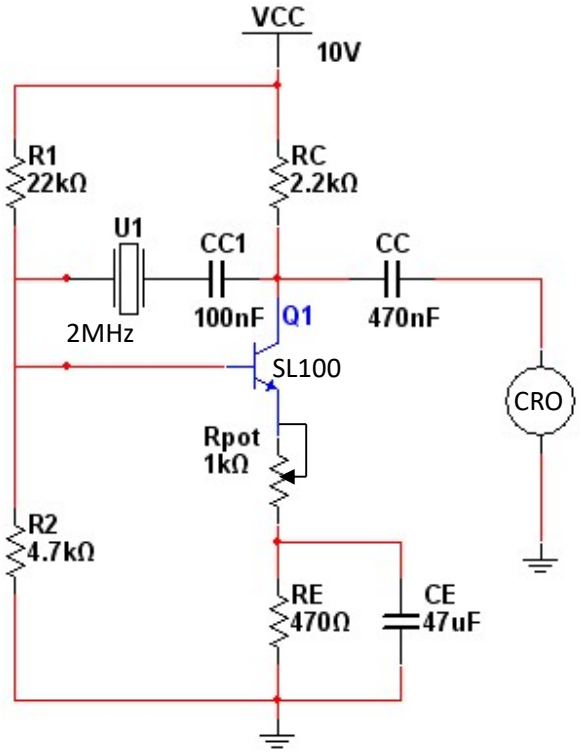


Fig.7.1: Crystal Oscillator

Procedure:

1. The amplifier circuit is rigged up as shown in the diagram and the DC condition is checked. i.e., V_{CE} = 5V
2. Also observe the wave form across the output using CRO
3. If wave is not observed, adjust the variable 1K pot in series with R_E resistor, until an undistorted sine wave is obtained.
4. Draw the waveform on the graph sheet and note down the frequency.

Expected output:

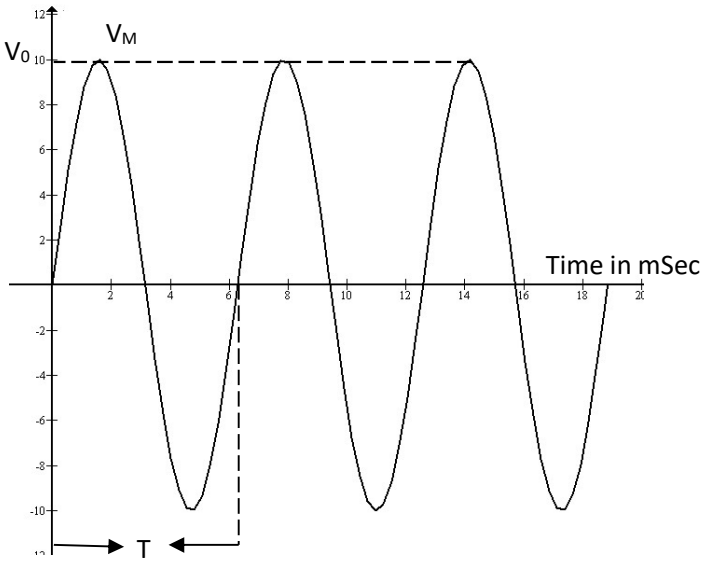


Fig.7.2: 2MHz output

Observations:

Time: ……mSec

Frequency:……Hz

Result:

Thus the performance of BJT – crystal Oscillators for RF range $f_0 \geq 100KHz$ is studied.

8.1 Second Order Butterworth Active Low Pass Filter

Aim: To design a Second order Active Low-pass Filter using Operational Amplifier for the given cut-off frequency and to determine Roll-off from its frequency response.

Components Required: Resistors-10kΩ, 15.9kΩ, 5.8kΩ Capacitors-0.01μF Op-Amp-μA741, Function Generator, connecting wires, spring board, Bread board, CRO

Circuit Diagram:

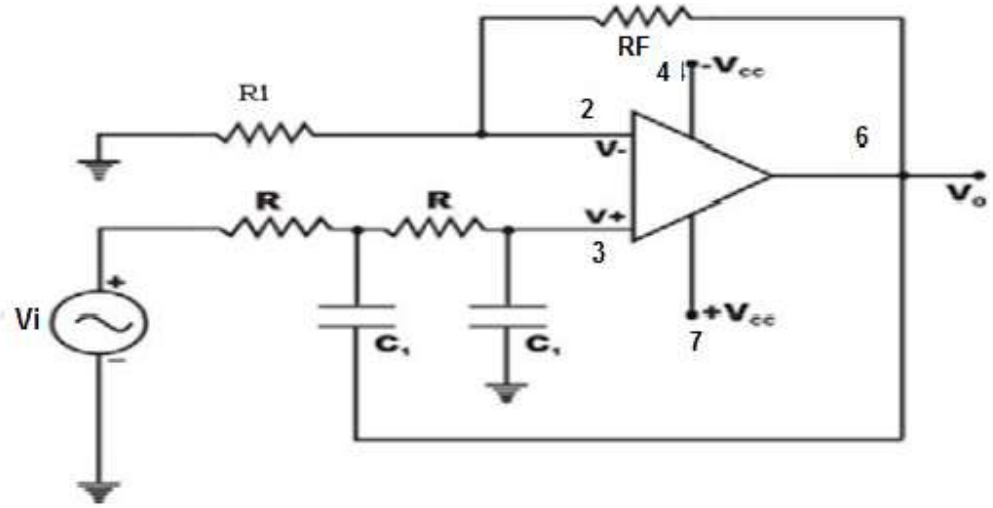


Fig.8.1: Second-Order Butterworth active low-pass filter

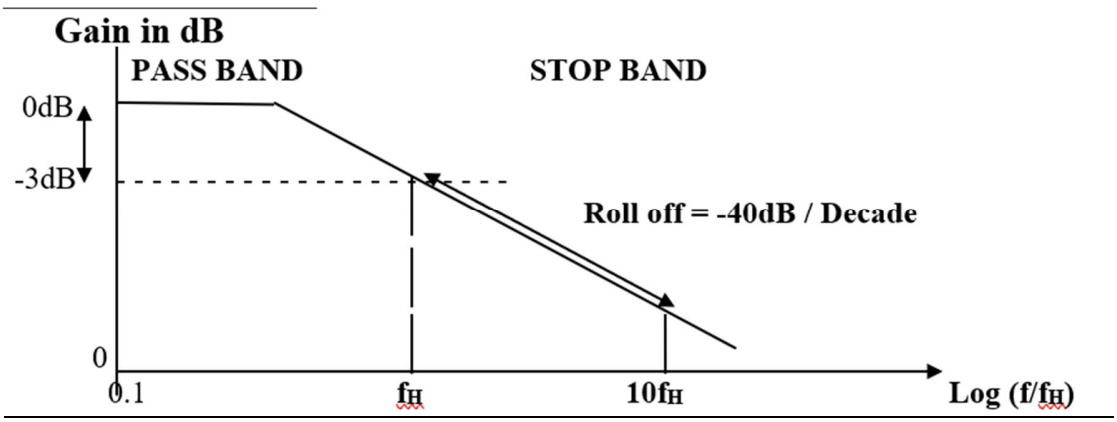
Design:

1. High cut-off frequency f_H for second order LPF is $f_H = \frac{1}{2\pi\sqrt{R2R3C2C3}}$
2. Let **f_H =1 kHz**. , **R_2=R_3=R** and **C_2=C_3=C=0.01μF.**
3. Therefore **R =1 / (2πf_HC) = 15.9kΩ.**
4. Pass-band voltage gain **A_F =3-α =3-1.414 = 1.586** where Damping coefficient **α=1.414** for II order filter
5. **Let R_1= 10KΩ** , Calculate **R_F** from **A_F = 1+ (R_F/ R_1)**
6. **Therefore R_F =0.586R_1. = 5.8KΩ**

Procedure:

1. Connections are made as shown in the circuit diagram. Apply sine wave input signal of peak amplitude 2 volts (Vi)
2. Keep Input signal (Vi) amplitude constant and vary the frequency from 100Hz to 50 kHz.& Note down the corresponding values of output voltage (Vo)
3. Calculate gain in dB using formula 20log 10(Vo / Vi)
4. Plot frequency versus Gain in dB in the Semi log sheet and mark fH.
5. Find the Roll-off factor from the graph = {Gain at 10fH} – {Gain at fH}.

Frequency Response:



Tabular column: V_i = 2V

Frequency	Output voltage (V_0)	Gain in dB= 20 log (Vo/Vi)
100Hz		
200Hz		
400Hz		
600Hz		
800Hz		
900Hz		
950Hz		
1KHz		
1.1KHz		
1.2KHz		
2KHz		
5kHz		
10KHz		
20KHz		
50KHz		

Result

	Higher Cut off Frequency	Roll-Off Factor
Theoretical		
practical		

Second Order Butterworth Active High Pass Filter

Aim: To design a Second Order Active High-pass Filter using Operational Amplifier for the given cut-off frequency and to determine Roll-off from its frequency response.

Components Required: Resistors-10kΩ, 15.9kΩ, 5.8kΩ**,** Capacitors-0.01μF**,** Op-amps-μA741**,** Frequency generator, connecting wires, spring board/bread board **&** CRO.

Circuit Diagram

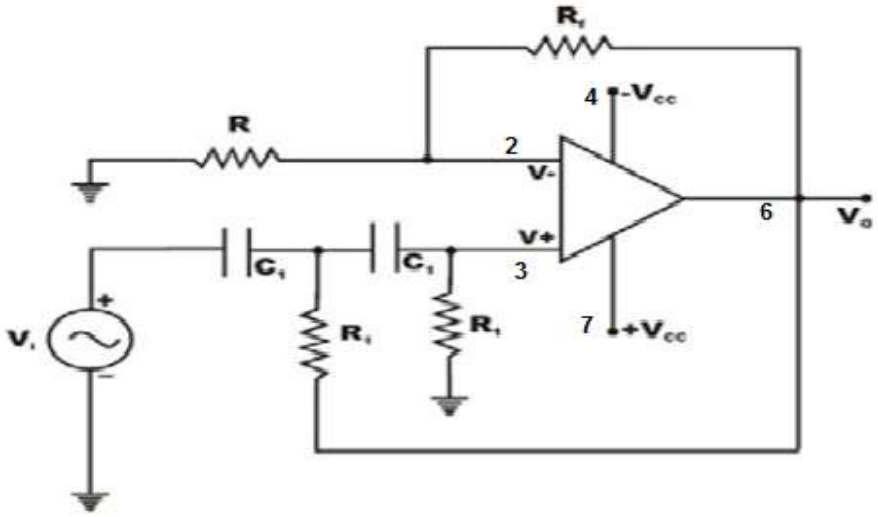


Fig 8. 2 Second-Order Butterworth Active High-Pass Filter

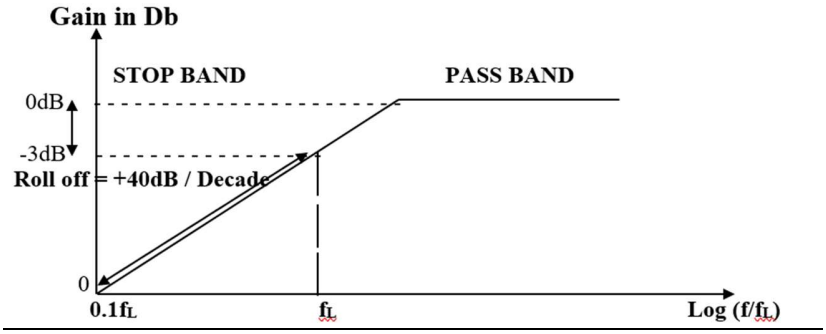
Design

1. Lower Cut-off frequency $\mathbf{f_L}$ for second order LPF is $f_L = \frac{1}{2\pi\sqrt{R2R3C2C3}}$
2. Let $\mathbf{f_L = 1\ kHz}$. , $\mathbf{R_2=R_3=R}$ and $\mathbf{C_2=C_3=C=0.01\mu F.}$
3. Therefore $\mathbf{R = 1 / (2\pi f_H C) = 15.9k\Omega.}$
4. Pass-band gain $\mathbf{A_F = 3-\alpha = 3-1.414 = 1.586}$ (Where Damping coefficient $\boldsymbol{\alpha = 1.414}$ for II order filter)
5. $\mathbf{A_F = 1+ (R_F/ R_1)}$ therefore $\mathbf{R_F = 0.586R_1}$. (where $\mathbf{A_F}$ is the pass band voltage gain of filter)
6. Let $\mathbf{R_1 = 10K\Omega}$, then $\mathbf{R_F = 0.586R_1 = 5.8k\Omega}$

Procedure:

1. Connections are made as shown in the circuit diagram. Apply sine wave input signal of peak amplitude 2 volts (Vi)
2. Keep Input signal (Vi) amplitude constant and vary the frequency from 100Hz to10 kHz.& Note down the corresponding values of output voltage (Vo)
3. Calculate gain in dB using formula 20log 10(Vo / Vi)
4. Plot frequency versus Gain in dB in the Semi log sheet and mark fL.
5. Find the Roll-off factor from the graph = {Gain at fL} – {Gain at 0.1fL}

Frequency Response:



Tabular column: V_i = 2V

Frequency	Output voltage (V_0)	Gain in dB= 20 log (Vo/Vi)
100Hz		
200Hz		
400Hz		
600Hz		
800Hz		
900Hz		
950Hz		
1KHz		
1.1KHz		
1.2KHz		
2KHz		
5kHz		
10KHz		
20KHz		

Result

	Higher Cut off Frequency	Roll-Off Factor
Theoretical		
practical		

9. R-2R Ladder Network for DAC

Aim: To design and test R-2R ladder network for DAC using op-amp µA741.

Components and equipments required:

Resistors-2KΩ, 1kΩ , Op-amps-µA741, Frequency generator, connecting wires, power supply.

Circuit Diagram:

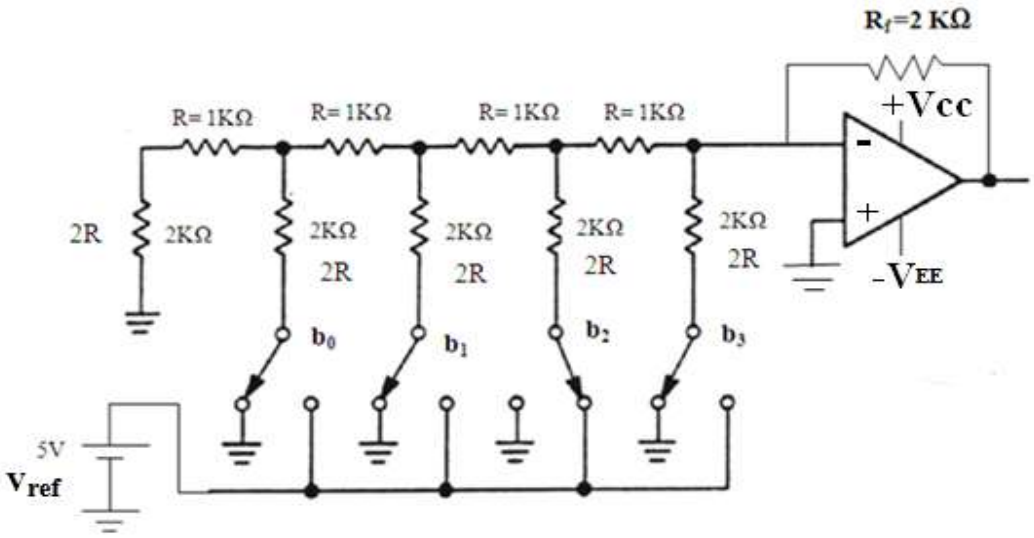


Fig 9 R-2R Ladder Network for DAC

Design Procedure:

Analog output voltage Vo theoretical values are calculated using the equation

$$Vo = -R_F \left[\frac{b_3}{2R} + \frac{b_2}{4R} + \frac{b_1}{8R} + \frac{b_0}{16R} \right]$$

Procedure:

1. Connections are made as shown in the circuit diagram.

2. Binary inputs (from 0 to 15) is applied and corresponding output voltage is measured using Multimeter.

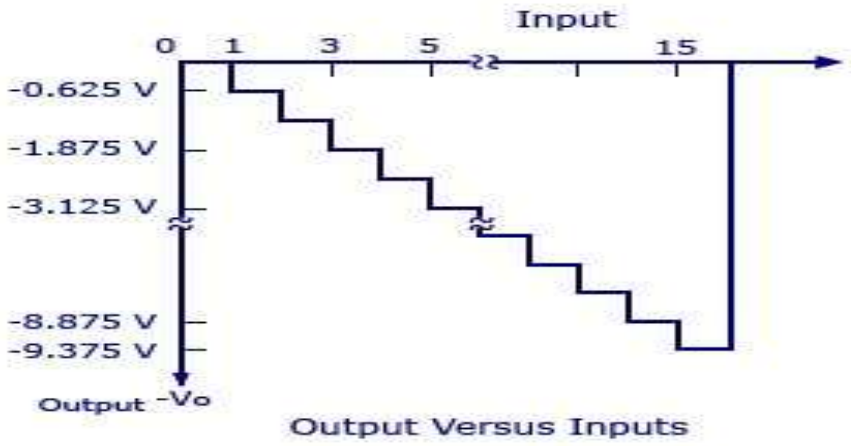
3. Theoretical values and Practical values of output are compared.

4. Plot the graph with decimal equivalent of binary inputs along X-axis and output voltage V0 along y-axis. Observe the staircase waveform or the ladder graph.

Tabular Column:

Decimal equivalent of binary inputs	Inputs (V) b_3 b_2 b_1 b_0				Analog output voltage value V_0	
					Theoretical	**Practical**
0	0	0	0	0	0	
1	0	0	0	5	-0.625	
2	0	0	5	0	-1.250	
3	0	0	5	5	-1.875	
4	0	5	0	0	-2.500	
5	0	5	0	5	-3.125	
6	0	5	5	0	-3.750	
7	0	5	5	5	-4.375	
8	5	0	0	0	-5.000	
9	5	0	0	5	-5.625	
10	5	0	5	0	-6.250	
11	5	0	5	5	-6.875	
12	5	5	0	0	-7.500	
13	5	5	0	5	-8.125	
14	5	5	5	0	-8.875	
15	5	5	5	5	-9.375	

Graph:



Output Versus Inputs

Result:

The practical values of output voltage V0 are approximately equal to theoretical values. The staircase waveform for outputs V/s inputs is plotted.

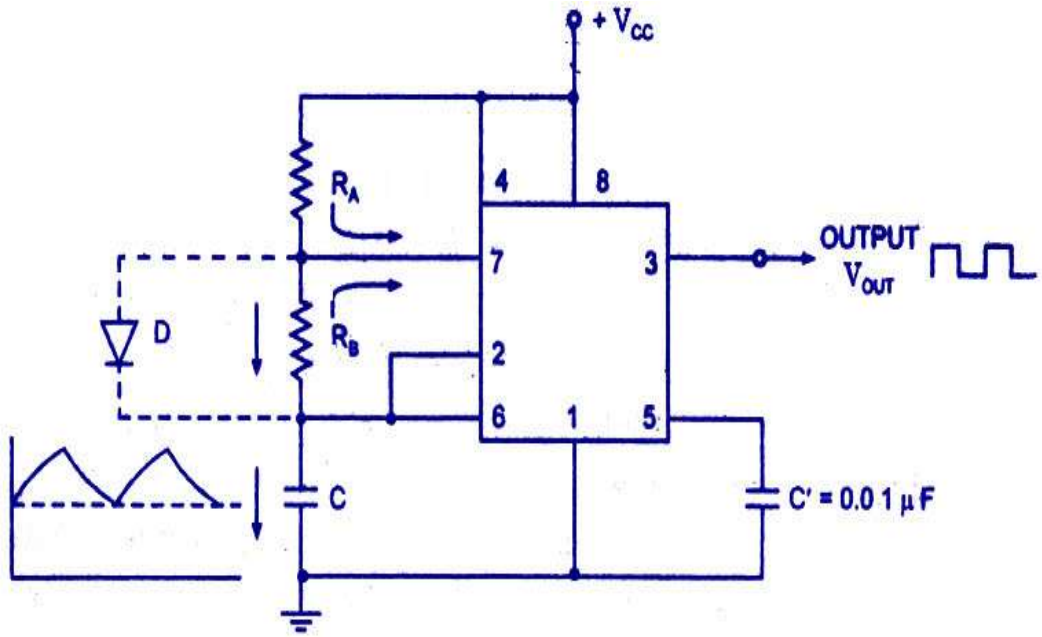
10. Design and Test Monostable and Astable Multivibrator using 555 Timer.

Aim: To design and verify the operation of Astable Multivibrator using IC 555 Timer for given frequency and duty cycle.

Components and equipments required:

Resistors-6.8KΩ, 3.4kΩ, 4.7kΩ, 4.9kΩ, 1.5kΩ
Capacitors-0.1μF
IC-555
Frequency generator, connecting wires, DC power supply, CRO

Circuit Diagram:



Circuit of The Timer 555 as an Astable Multivibrator

Fig 10.1 Astable Multivibrator Using Ic-555 Timer

Design:

For an astable multivibrator,

$T_{ON} = 0.693(R_A + R_B)\ C$ and $T_{OFF} = 0.693R_BC$

Total Time Period, $T = T_{ON}+T_{OFF}$

So, $T = 0.693(R_A + 2R_B)\ C$

Frequency of Oscillations, $F=1/T=1.45/ [(R_A + 2R_B)\ C]$

Duty cycle = $T_{ON}/T= (R_A + R_B)/ (R_A + 2R_B)$

For given value of duty cycle 75%,

$(R_A + R_B)/ (R_A + 2R_B)=0.75$

$R_A + R_B = 0.75R_A + 1.5R_B$

$R_A = 2R_B$. Let $R_A = 6.8k\Omega$. Then, $R_B = 3.4k\Omega$

Given F = 1kHz then from (1), $1kHz = 1.45/ [(R_A + 2R_B)C]$

Let $C = 0.1\mu F$. Then, $R_A + 2R_B = 14.5k$

Let $R_A = 4.7k\Omega$ (standard value). Then, $R_B = 4.9k\Omega$

For duty cycle=80%

$R_A + 2R_B = 0.8$

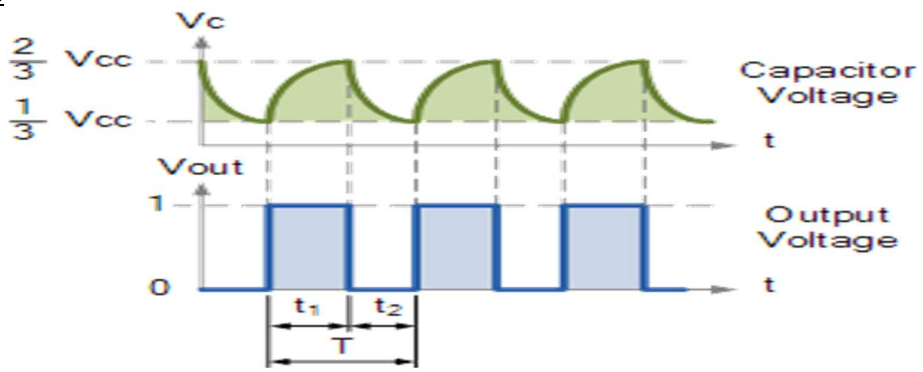
$R_A + R_B = 0.8\ R_A + 1.6R_B$

$R_A = 3R_B$. Let $R_A = 4.7k\Omega$. Then, $R_B = 1.5k\Omega$

Procedure:

1. Connections are made as shown in the circuit diagram
2. Switch on the DC power supply unit
3. Observe the wave form on CRO at pin 3 and measure the o/p pulse amplitude
4. Observe the wave form on CRO at pin 6 and measure Vcmax and Vc min
5. Verify that Vcmax=2/3Vcc and Vc min=1/3 Vcc.
6. Calculate the duty cycle D, o/p frequency and verify with specified value.

Waveforms:



Observation And Calcualtion:

Tabular Column:

R_A	R_B	C	F (Theoretical)	T_{ON}	T_{OFF}	T	F (Practical)	Duty Cycle

Result:

The working of astable multivibrator is verified for different duty cycles of operation.

MONOSTABLE MULTIVIBRATOR USING IC-555 TIMER

Aim: To design and verify the operation of a Monostable Multivibrator using IC 555 Timer for given pulse width.

Components required:

Resistors-10kΩ

Capacitors-0.1μF

IC-555

Frequency generator, connecting wires, DC power supply, CRO

Circuit Diagram:

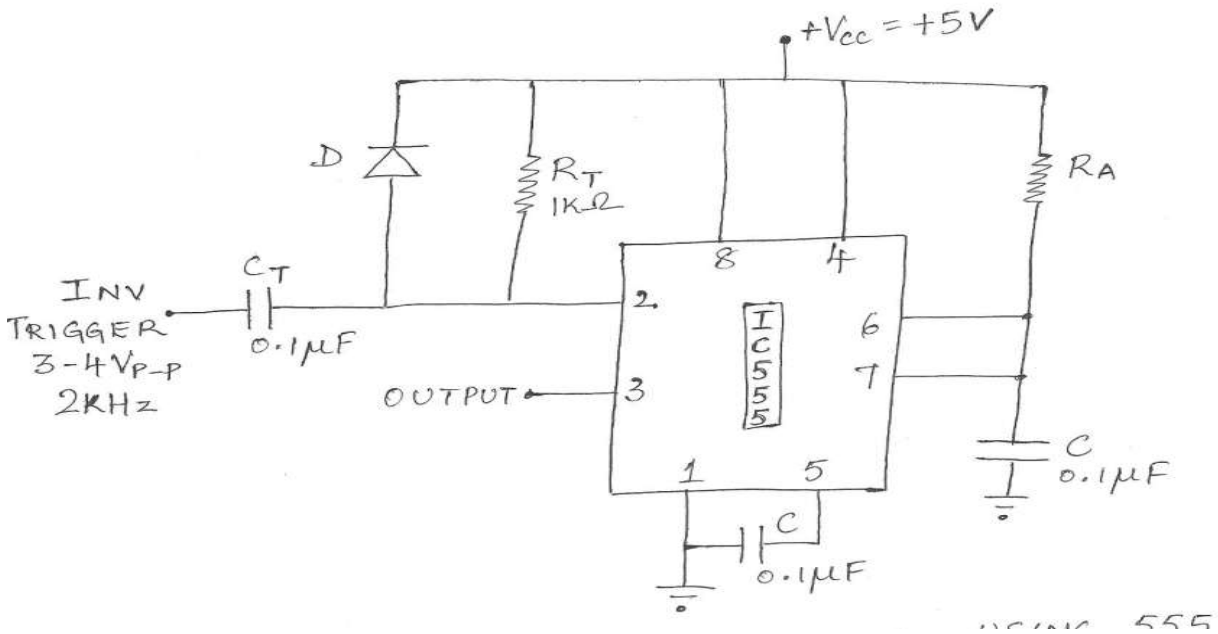


Fig 10.2 Monostable Multivibrator Using Ic-555 Timer

Design:

Given Tp = 1ms

F = 1 kHz

$Tp = 1.1R_AC$

Let C = 0.1μF

$R_A = (1*10^{-3}) / (1.1*0.1*10^{-6})$

R_A = 9.09 kΩ (use 10kΩ standard value)

For differentiator, R_TC_T=10μs

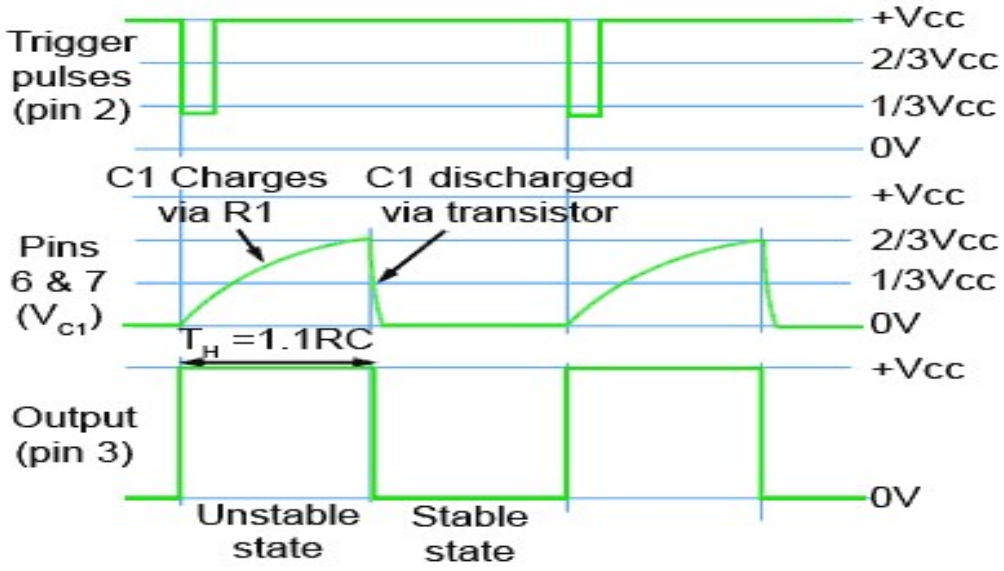
Assume C_T=0.1μF

So, R_T=1kΩ

Procedure:

1. Rig up the circuit as shown in the figure after checking all the components.
2. Apply suitable inputs to the monostable multivibrator (DC & Trigger inputs). Normally inverting trigger of 3 to 4Vp-p is applied with a frequency of 2kHz.
3. Observe the waveform across the timing capacitor in one channel and the output in the other channel.
4. Verify the designed values and the repeat the above procedure for different set of values.

Waveforms:



:

TABULAR COLUMN

R	C	Tp = 1.1RC	Tp(prac)

Result:

The working of Monostable multivibrator is verified for different duty cycles of operation.